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FREESCALE SEMICONDUCTOR, INC.
LAW DEPARTMENT
7700 WEST PARMER LANE MD:TX32/PL02
AUSTIN, TX 78729

EXAMINER	
GUILL, RUSSELL L	
ART UNIT	**PAPER NUMBER**
2123	

DATE MAILED: 11/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/942,166	BLAAUW ET AL.
	Examiner	Art Unit
	Russell L. Guill	2123

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _15 August 2005_.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-33_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _15 August 2005_ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to an Amendment filed August 15, 2005. Claims 1 - 2, 14, 22 - 23 and 29 have been amended. No claims have been canceled. Claims 1 - 33 have been examined. Claims 1 - 33 have been rejected.

Response to Remarks

2. Regarding the objection to the drawings, the drawings were received on August 15, 2005. These drawings are acceptable.

3. Regarding the rejection of claims 1 and 14 under 35 USC § 101, the Applicant's amendments to the claims overcome the rejection, and accordingly, the rejection is withdrawn.

4. Regarding the rejection of independent claims 1, 14, 22 and 29, the Applicant argues that in the claims, as amended, that the examiner's reference to Burks (column 9, lines 30 - 36) does not teach generating a before transition function and an after transition function corresponding to the predetermined input transition and predetermined output transition. The examiner respectfully disagrees, as explained in the following paragraphs.

5. The cited lines include an equation:

$$l_Y(X=1) \bullet \overline{h_Y(X=1)} \bullet \overline{l_Y(X=0)}$$

6. It would have been obvious to an ordinary artisan at the time of invention that this equation consists of a portion that represents that before the input transition has occurred, the output must not be pulled to the desired state:

(1) $$\overline{l_Y(X=0)}$$

which corresponds to the Applicant's before transition function $G_{before} = \overline{L}_{X|A=0}$ (by substituting the corresponding variables from equation 1 above).

7. Further, it would have been obvious to an ordinary artisan at the time of invention that this equation also consists of a portion that represents that after the input transition has finished, the output must be pulled to the desired state, and further the output must not be pulled to the opposite of the desired state:

(2) $$l_Y(X=1) \bullet \overline{h_Y(X=1)}$$

which corresponds to the Applicant's after transition function $G_{after} = L_{X|A=1} * \overline{H}_{X|A=1}$ (by substituting the corresponding variables from equation 2 above).

8. Therefore, the cited Burks reference appears to teach generating a before transition function and an after transition function corresponding to the predetermined input transition and predetermined output transition. Accordingly, the rejections of claims 1 - 33 are maintained.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. **Claims 1, 14, 15, 22 and 29** are rejected under 35 U.S.C. 103(a) as being unpatentable over Burks (U.S. Patent Number 5,946,475) in view of Bryant (Bryant, Randal E.; McDonald, Clayton B.; "CMOS Circuit Verification With Symbolic Switch-Level Timing Simulation", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Volume 20, Number 3, March 2001).

10.1. **Regarding claim 1**, Burks teaches:

10.1.1. A method for generating a switching vector (**column 8, lines 61 - 67; and column 9, lines 1 - 10**);

10.1.2. providing a circuit having a transitioning input which receives a predetermined input transition, side inputs which assume side states, an output which provides a predetermined output transition in response to the predetermined input transition and the side states (**figure 1; and column 8, lines 29 - 67; and column 9, lines 1 - 35**), and an internal node (**figure 2, node labeled Y**), wherein the internal node is a node located within a feedback path of the circuit (**figure 1, nodes Y and Z form a feedback path**).

10.1.3. generating a Boolean transition function which represents the side states of the side inputs that cause the predetermined output transition to occur (**column 9, lines 10 - 35**) wherein generating the Boolean transition function comprises generating a before transition function and an after transition function corresponding to the predetermined input transition and predetermined output transition (**column 9, lines 1 - 36**);

10.1.4. using a switching vector generator, determining the switching vector which satisfies the Boolean transition function (**column 9, lines 26 - 35**).

10.2. **Regarding claim 1,** Burks does not specifically teach:

10.2.1. providing a circuit having a transitioning input which receives a predetermined input transition, side inputs which assume side states, an output which provides a predetermined output transition in response to the predetermined input transition and the side states, and an internal node, wherein the internal node is at least one of a node located within a feedback path of the circuit ***and a node capable of assuming a first state, a second state, and a third state***.

10.3. **Regarding claim 1,** Bryant teaches:

10.3.1. and a node capable of assuming a first state, a second state, and a third state (**figure 18 (a); and page 468, section G. Ternary Simulation**).

10.4. **Regarding claim 14,** Burks teaches:

10.4.1. A method for generating a set of switching vectors (**column 8, lines 61 - 67; and column 9, lines 1 - 10**);

10.4.2. providing a circuit having a transitioning input which receives a predetermined input transition, side inputs which assume side states, an output which provides a predetermined output transition in response to the predetermined input transition and the side states (**figure 1; and column 8, lines 29 - 67; and column 9, lines 1 - 35**), and a plurality of internal nodes (**figure 2, node labeled Y; it would have been obvious to have a plurality of internal nodes**), wherein each of the plurality of internal nodes is at least one of a node located within a feedback path of the circuit (**figure 1, nodes Y and Z form a feedback path**).

10.4.3. using a switching vector generator, determining the set of switching vectors corresponding to the side states which results in the predetermined output transition, wherein the set of switching vectors is a subset of a full enumeration of all side states for the circuit **(column 9, lines 10 - 35)**, and wherein determining the switching vector includes generating a before transition function and an after transition function corresponding to the predetermined input transition and predetermined output transition **(column 9, lines 1 - 36)**;

10.5. **Regarding claim 14**, Burks does not specifically teach:

10.5.1. providing a circuit having a transitioning input which receives a predetermined input transition, side inputs which assume side states, an output which provides a predetermined output transition in response to the predetermined input transition and the side states, and a plurality of internal nodes, wherein each of the plurality of internal nodes is at least one of a node located within a feedback path of the *circuit and a node capable of assuming a first state, a second state, and a third state*;

10.6. **Regarding claim 14**, Bryant teaches:

10.6.1. a node capable of assuming a first state, a second state, and a third state **(figure 18 (a); and page 468, section G. Ternary Simulation)**.

10.7. **Regarding claim 15**, Burks teaches:

10.7.1. The set of switching vectors include only those switching vectors that result in the predetermined output transition **(column 8, lines 61 - 67; and column 9, lines 1 - 38)**.

10.8. **Regarding claim 22**, Burks teaches:

10.8.1. A switching vector generator stored via at least one computer readable medium storing instructions executable by a computer **(column 16, lines 1 - 15)**;

10.8.2. a first set of instructions for receiving a circuit having a transitioning input which receives a predetermined input transition, side inputs which assume side states, an output which provides a predetermined output transition in response to the predetermined input transition and the side states **(figure 1; and column 8, lines 29 - 67; and column 9, lines 1 - 35; and column 16, lines 1 - 15)**, and an internal node **(figure 2, node labeled Y)**, wherein the internal node is at least one of a node located within a feedback path of the circuit **(figure 1, nodes Y and Z form a feedback path)**.

10.8.3. a second set of instructions for generating a Boolean transition function which represents the side states of the side inputs that cause the predetermined output transition to occur (**column 9, lines 10 - 35; and column 16, lines 1 - 15**); and

10.8.4. a third set of instructions for determining the switching vector which satisfies the Boolean transition function (**column 9, lines 26 - 35; and column 16, lines 1 - 15**); and

10.8.5. a fourth set of instructions for generating a before transition function and an after transition function corresponding to the predetermined input transition and predetermined output transition (**column 9, lines 1 - 36**).

10.9. **Regarding claim 22**, Burks does not specifically teach:

10.9.1. a first set of instructions for receiving a circuit having a transitioning input which receives a predetermined input transition, side inputs which assume side states, an output which provides a predetermined output transition in response to the predetermined input transition and the side states, and an internal node, wherein the internal node is at least one of a node located within a feedback path of the circuit <u>***and a node capable of assuming a first state, a second state, and a third state***</u>;

10.10. **Regarding claim 22**, Bryant teaches:

10.10.1. a node capable of assuming a first state, a second state, and a third state (**figure 18 (a); and page 468, section G. Ternary Simulation**).

10.11. **Regarding claim 29**, Burks teaches:

10.11.1. A switching vector generator stored via at least one computer readable medium storing instructions executable by a computer (**column 16, lines 1 - 15**);

10.11.2. a first set of instructions for receiving a circuit having a transitioning input which receives a predetermined input transition, side inputs which assume side states, an output which provides a predetermined output transition in response to the predetermined input transition and the side states (**figure 1; and column 8, lines 29 - 67; and column 9, lines 1 - 35; and column 16, lines 1 - 15**), and a plurality of internal nodes (**figure 2, node labeled Y; it would have been obvious to have a plurality of internal nodes**), wherein each of the plurality of internal nodes is at least one of a node located within a feedback path of the circuit (**figure 1, nodes Y and Z form a feedback path**).

10.11.3. a second set of instructions for determining the set of switching vectors corresponding to the side states which results in the predetermined output transition, wherein the set of switching vectors is a subset of a full enumeration of all side states for the circuit (**column 9, lines 10 - 35**), and wherein determining the set of switching vectors includes generating a before transition function and an after transition function corresponding to the predetermined input transition and predetermined output transition (**column 9, lines 1 - 36**);

10.12. **Regarding claim 29**, Burks does not specifically teach:

10.12.1. a first set of instructions for receiving a circuit having a transitioning input which receives a predetermined input transition, side inputs which assume side states, an output which provides a predetermined output transition in response to the predetermined input transition and the side states, and a plurality of internal nodes, wherein each of the plurality of internal nodes is at least one of a node located within a feedback path of the circuit and ***a node capable of assuming a first state, a second state, and a third state***;

10.13. **Regarding claim 29**, Bryant teaches:

10.13.1. a node capable of assuming a first state, a second state, and a third state (**figure 18 (a); and page 468, section G. Ternary Simulation**).

10.14. The motivation to use the art of Bryant with the art of Burks would have been the benefit recited in Bryant of providing real-valued data dependent delay values applied in timing and functional verification of CMOS transistor circuitry (**page 458, Abstract**). Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Bryant with the art of Burks to produce the claimed inventions.

11. **Claims 2 - 13, 16 - 21, 23 - 28 and 30 - 33** are rejected under 35 U.S.C. 103(a) as being unpatentable over Burks and Bryant, in view of Parashkevov (Parashkevov, Atanas Nikolaev; European Patent Application EP 1 083 500 A2, "A method of analyzing a circuit having at least one structural loop within a channel connected component").

11.1. **Regarding claims 16 and 30**, Burks teaches:

11.1.1. A method for generating a before transition function and an after transition function corresponding to the predetermined input transition and predetermined output transition (**column 9, lines 30 - 36**);

11.2. **Regarding claims 2, 16, 23 and 30,** Burks teaches:

11.2.1. selecting a first term within one of the before transition function or the after transition function, wherein the first term is expressed as a function of the internal node **(column 9, lines 47 - 63; it would have been obvious to select a first term, as the formulas for h_y and l_y were obviously obtained through an expansion process)**;

11.2.2. Using an expansion equation to generate the Boolean transition function **(column 10, lines 10 - 63)**.

11.3. **Regarding claims 2, 16, 23 and 30,** Burks does not specifically teach:

11.3.1. expanding the first term with respect to the internal node to obtain an expansion equation.

11.3.2. Using the expansion equation to reduce the transition function with respect to the at least one internal node to obtain a reduced transition function.

11.4. **Regarding claims 2, 16, 23 and 30,** Parashkevov teaches:

11.4.1. expanding a term with respect to an internal node to obtain an expansion equation **(figure 4, element 402; paragraph 0036)**.

11.4.2. reducing the expansion equation with respect to the at least one internal node **(figure 4, element 402; paragraph 0036)**.

11.5. The motivation to use the art of Parashkevov with the art of Burks would have been the benefits recited in Parashkevov that the provided method of analyzing a circuit with a structural loop within a channel connected component (CCC) overcomes or reduces the problems with the existing methods which either introduce a potentially large number of nets in an unknown state or completely ignore the problem **(paragraphs 0009, 0007)**. This is an important benefit given that a key aspect in deriving a functional model of a single CCC is the ability to identify and properly characterize the behavior introduced by structural dependency loops within CCC's **(paragraph 0006)**. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Parashkevov with the art of Burks to produce the claimed inventions.

11.6. **Regarding claims 3 and 24,** Burks teaches:

11.6.1. Generating the Boolean transition function further comprises substituting the first term with the expansion equation (**column 9, lines 1 - 63; column 10, lines 10 - 30**).

11.7. **Regarding claims 4 and 25,** Burks does not specifically teach:

11.7.1. That an expansion equation defines a reduction value for an internal node.

11.8. **Regarding claims 4 and 25,** Parashkevov teaches:

11.8.1. That an expansion equation defines a reduction value for an internal node (**figure 4, element 402; paragraphs 0022, 0023, 0036**).

11.9. **Regarding claims 5, 19, 26 and 31,** Burks teaches:

11.9.1. selecting a second term within one of the before transition function or the after transition function, wherein the second term is expressed as a function of the internal node (**column 9, lines 1 - 63; please note that in order to form the expression on line 56, that the terms had to be expanded; column 10, lines 10 - 30; it would have been obvious to use an internal node**).

11.9.2. substituting an expanded value for the internal node in the second term node (**column 9, lines 1 - 63; please note that in order to form the expression on line 56, that the terms had to be expanded; column 10, lines 10 - 30; it would have been obvious to use an internal node**).

11.10. **Regarding claims 5, 19, 26 and 31,** Burks does not specifically teach:

11.10.1. substituting ***the reduction value*** for the internal node in the second term.

11.11. **Regarding claims 5, 19, 26 and 31,** Parashkevov teaches:

11.11.1. substituting the reduction value for the internal node (**paragraphs 0022, 0023, 0036**).

11.12. **Regarding claims 6, 20, 27 and 32,** Burks teaches:

11.12.1. an internal node capable of assuming the first state and the second state (**figure 1, node Y**).

11.13. **Regarding claims 6, 20, 27 and 32,** Burks does not specifically teach:

11.13.1. The method of claim 3, wherein the internal node is capable of assuming the first state, the second state***, and the third state, the third state being a different state from the first state and the second state and wherein the expansion equation comprises:***

11.13.2. *a first term corresponding to the internal node assuming the first state;*

11.13.3. *a second term corresponding to the internal node assuming the second state; and*

11.13.4. *a third term corresponding to the internal node assuming the third state*

11.14. **Regarding claims 6, 20, 27 and 32,** Bryant teaches:

11.14.1. a node is capable of assuming the first state, the second state, and the third state, the third state being a different state from the first state and the second state (**page 468, section G. Ternary Simulation**).

11.15. **Regarding claims 6, 20, 27 and 32,** Parashkevov teaches:

11.15.1. an expansion equation comprises:

11.15.2. a first term corresponding to the internal node assuming the first state (**figure 4, element 402; paragraph 0036**).

11.15.3. a second term corresponding to the internal node assuming the second state (**figure 4, element 402; paragraph 0036**).

11.15.4. a third term corresponding to the internal node assuming the third state (**figure 4, element 402; paragraph 0036; it would have been obvious to have a third term for a third state**).

11.16. **Regarding claims 7, 21, 28 and 33,** Burks does not specifically teach:

11.16.1. the first state comprises logic high state, the second state comprises a logic low state, and the third state comprises at least one of an unknown state, a high impedance state, and a short circuit state.

11.17. **Regarding claims 7, 21, 28 and 33,** Bryant teaches:

11.17.1. the first state comprises logic high state, the second state comprises a logic low state, and the third state comprises at least one of an unknown state, a high impedance state, and a short circuit state (**page 468, section G. Ternary Simulation**).

11.18. **Regarding claim 8,** Burks teaches:

11.18.1. generating a Boolean transition function further comprises:

11.18.1.1. selecting a second term within one of the before transition function or the after transition function, wherein the first term is expressed as a function of the second internal node (**column 9, lines 47 - 63; it would have been obvious to select a second term, as the formulas for h_y and l_y were obviously obtained through an expansion process**).

11.18.1.2. expanding the second term with respect to the second internal node to obtain an expansion equation (**column 9, lines 47 - 63; it would have been obvious to expand a second term, as the formulas for h_y and l_y were obviously obtained through an expansion process**); and

11.18.1.3. substituting the second term with the expansion equation (**column 9, lines 47 - 63; it would have been obvious to substitute a second term with an expansion equation, as the formulas for h_y and l_y were obviously obtained through an expansion process**).

11.19. **Regarding claim 8,** Burks does not specifically teach:

11.19.1. The method of claim 3, wherein the circuit includes a second internal node, wherein the second internal node is at least one of a node located within a feedback path of the circuit and a node capable of assuming a first state, a second state, and a third state.

11.20. **Regarding claim 8,** Bryant teaches:

11.20.1. a node capable of assuming a first state, a second state, and a third state (**page 468, section G. Ternary Simulation**).

11.21. **Regarding claim 8,** Parashkevov teaches:

11.21.1. a circuit includes a second internal node, wherein the second internal node is at least one of a node located within a feedback path of the circuit (**figure 4, element 402; paragraphs 0022, 0023, 0036**).

11.22. **Regarding claim 9,** Burks does not specifically teach:

11.22.1. when the expansion equation is satisfied, the first term is satisfied.

11.23. **Regarding claim 9,** Parashkevov teaches:

11.23.1. when the expansion equation is satisfied, the first term is satisfied (**figure 4, element 402; paragraph 0036**).

11.24. **Regarding claim 10**, Burks teaches:

11.24.1. That the output and the internal node is the same node (**figure 1, node Y; and column 9, lines 10 - 25 where node Y is the output node**).

11.25. **Regarding claim 11**, Burks teaches:

11.25.1. That the internal node is located within the feedback path of the circuit (**figure 1, nodes Y and Z form a feedback path**).

11.26. **Regarding claim 12**, Burks teaches:

11.26.1. The internal node is capable of assuming the first state and the second state (**figure 1, node Y**).

11.27. **Regarding claim 12**, Burks does not specifically teach:

11.27.1. The internal node is capable of assuming the first state, the second state, ***and the third state***.

11.28. **Regarding claim 12**, Bryant teaches:

11.28.1. a node is capable of assuming the first state, the second state, and the third state (**page 468, section G. Ternary Simulation**).

11.29. **Regarding claim 13**, Burks teaches:

11.29.1. The internal node is located within the feedback path of the circuit and is capable of assuming the first state and the second state (**figure 1, nodes Y and Z).**

11.30. **Regarding claim 13**, Burks does not specifically teach:

11.30.1. The internal node is located within the feedback path of the circuit and is capable of assuming the first state, the second state, ***and the third state***.

11.31. **Regarding claim 13**, Bryant teaches:

11.31.1. a node is capable of assuming the first state, the second state, and the third state (**page 468, section G. Ternary Simulation**).

11.32. **Regarding claim 17**, Burks teaches:

11.32.1. The reduced transition function is not expressed as a function of any of the plurality of internal nodes (**column 9, lines 47 - 62**).

11.33. **Regarding claim 18,** Burks teaches:

11.33.1. The set of switching vectors satisfies the reduced transition function (**column 9, lines 47 - 62**).

11.34. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Parashkevov with the art of Burks to produce the claimed inventions.

Conclusion

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

13. **Examiner's Note:** Examiner has cited particular columns and line numbers in the references applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in their entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Russell L. Guill whose telephone number is 571-272-7955. The examiner can normally be reached on Monday - Friday 10:00 AM - 6:30 PM.

15. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Picard can be reached on 571-272-3749. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Any inquiry of a general nature or relating to the status of this application should be directed to the TC2100 Group Receptionist: 571-272-2100.

16. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Russ Guill
Examiner
Art Unit 2123

RG

Paul P. Rodriguez 10/28/05
Primary Examiner
Art Unit 2125